ABSTRACT OF THE DISCLOSURE

A resampling technique is used to reduce the noise and improve the signal quality in the output of a prescaler circuit (10). The resampling of the output of a last frequency divider stage is accomplished using at least one flip/flop (FF) (e.g., a D-type FF 18) that is clocked by a signal obtained from the input of the prescaler. This reduces or eliminates the noise caused by edge jitter in the output of the prescaler, as well as the effect of spurious signals generated by the prescaler. These teachings can be used in integer N PLLs and in fractional N PLLs, as well as in single and programmable dual or multi-modulus prescalers. Using this technique the current consumption of the prescaler frequency dividers (12, 14, 16) need not be increased in an effort to reduce the prescaler noise., thereby conserving current in battery powered and other applications.